REMARKS

The present Amendment amends claims 1-16, 18-31, 36-39, 41 and 42. Therefore, the present application has pending claims 1-16, 18-31, 36-39, 41 and 42.

The title of the invention stands objected to as not being descriptive. The title of the invention was changed to "SCALABLE DISK ARRAY CONTROLLER" which Applicants submit is descriptive of the present invention. Therefore, Applicants submit that this objection is overcome and should be withdrawn.

In paragraph 3 of the Office Action the Examiner alleges that the lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The specification was extensively reviewed so as to uncover any minors that required correction. No other such minor errors were uncovered. Therefore, the Examiner's cooperation is respectfully requested to identify any errors the Examiner may be aware of so that such errors may be immediately corrected to expedite prosecution of the present application.

In paragraph 4 of the Office Action the Examiner objected to Figs. 2 and 3 as not being designated by the legend "Prior Art". Filed on even date herewith are Proposed Drawing Corrections adding the legend "Prior Art" to Figs. 2 and 3. Therefore, this objection is overcome and should be withdrawn.

In paragraph 5 of the Office Action the Examiner alleges that the "Oath/Declaration is defective because it does not provide a claim for domestic priority under 35 USC §120. This allegation by the Examiner is confusing since the present application was filed in the United States Patent and Trademark Office as the National Phase application of PCT International application No.

PCT/JP/98/02176. There is no claim in any of the papers filed with respect to the present application that another U.S. application is being relied upon for priority under 35 USC §120. 35 USC §120 concerns continuation applications not applications which have entered the National Phase in the United States Patent and Trademark Office based on an International PCT application.

Therefore, the Examiner is respectfully requested to clarify the allegation as set forth in paragraph 5 of the Office Action.

Claims 1-16, 18-31, 36-39, 41 and 42 stand rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regards as the invention. Various amendments were made throughout claims 1-16, 18-31, 36-39, 41 and 42 to bring them into conformity with the requirements of 35 USC §112, second paragraph. Therefore, Applicants submit that this rejection is overcome and should be withdrawn.

Specifically, amendments were made throughout the claims to overcome the objections noted by the Examiner in paragraphs 7-9 of the Office Action.

However, with respect to the Examiner's objection to the terms "package" and "platter" the following is provided.

The terms "package" and "platter" are well known in the art as evidenced by U.S. Patent No. 5,819,054 (Ninomiya). Generally, the word "package" means a circuit board on which a functional module is mounted (see col. 8, lines 3-25, and "CACHE 3", "HSTA 1", "DKA 2" or "CACHE PORT PACKAGE 22" in Fig. 7, of Ninomiya). On the other hand, the word "platter" means a back plane that is a circuit

board on which connectors to the "packages" are mounted, and moreover, on which the paths coupling the "packages" are printed (see col. 8, lines 3-25, "back plane 77" in Fig. 7 of Ninomiya).

Therefore, the term "package" in claims 1-12, defines the circuit board on which a channel interface module, a disk interface module or memory module is mounted (see Embodiments 1 or 17 of the present application and Figs. 75-78, 80-82). On the other hand, the term "platter" in claims 6, 7, 13-16, 18-31, 36-39, 41 and 42, defines the circuit board on which connectors to the channel interface packages, the disk interface packages or the memory packages are mounted, and moreover, on which the paths coupling these packages are printed, and on which a connector to the cable for coupling to another platter is mounted (see Embodiment 1, 17 of the present application and Figs. 75-78, 80-82).

The Examiner's cooperation is respectfully requested to contact Applicants' Attorney by telephone should any further indefinite matter be discovered so that appropriate amendments may be made.

Claims 1-15, 18-20, 22-31, 37 and 42 stand rejected under 35 USC §102(b) as being anticipated by Brant (U.S. Patent No. 5,887,270). This rejection is traversed for the following reasons. Applicants submit that the features of the present invention as now recited in claims 1-15, 18-20, 22-31, 37 and 42 are not taught or suggested by Brant whether taken individually or in combination any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

The features of the present invention as recited in each of the above noted claims are not taught or suggested by Brant whether taken individually or in combination any of the other references of record.

Particularly, the features of the present invention as recited in claims 1 and 8 are not taught or suggested by Brant. Claims 1 and 8 of the present application are each directed to a disk array controller comprising a channel interface package, a disk interface package, and memory package, wherein connections are made between the channel interface package and the memory package, and between the disk interface package and the memory package by cables. The term "package" means the circuit board on which a channel interface module, a disk interface module or a memory module is mounted respectively. Since the connections are made by cables, even if one package fails, only components for which the package is responsible have to be stopped and the defective package can be replaced without stopping the entire system. Thus, faults can be remedied without stopping the system so that the system can be operated without interruption around the clock, all the year round (see the first embodiment in the specification).

Brant, however, discloses a disk array controller comprising a channel interface device, a disk interface device and a memory devices, wherein connections are made between the channel interface device and the memory device, and between the disk interface device and the memory device by PCI buses or other paths (see Figs. 1, 3, col. 5, lines 17-56 in Brant). Thus, Brant merely discloses logical components and logical connections. Brant does not disclose physical components such as a "package" and/or a "cable" as recited in the claims.

Furthermore, Brant does not disclose the advantageous features of the present invention of making connections by "cables".

Therefore, the features of the present invention as recited in claims 1 and 8 are not anticipated nor rendered obvious by Brant.

Further, the features of the present invention as recited in claims 13, 18, 22, 27, 30, 37 and 42 are not taught or suggested by Brant whether taken individually or in combination any of the other references of record. Claims 13, 18, 22, 27, 30, 37 and 42 of the present application are each directed to a disk array controller comprising a channel interface package, a disk interface package, and a memory package, and plural platters on which one or plurality of the packages are mounted, wherein connections are made between the platters by cables, and wherein the path coupling the package to the cable is printed on each of the platters. The "package" means the circuit board on which a channel interface module or a disk interface module or memory module is mounted respectively, and the "platter" means the circuit board on which connectors to the packages are mounted, and on which the paths coupling these packages are printed, and further on which a connector to the cable for coupling to another platter is mounted. Since the connections are made by cables, even if one platter fails, only components for which the packages mounted on that platter are responsible have to be stopped and the defective part on the platter can be replaced without stopping the entire system. Thus, faults can be remedied without stopping the system so that the system can be operated without interruption around the clock, all the year round. Furthermore, to cope with the increase or decrease in the number of platters bearing interface packages, the

performance of internal buses can be made scalable. Therefore, scalability of performance and capacity is assured to suit a wide range of systems from small to large systems without unfavorably affecting cost performance. Further, it becomes possible to supply products at reasonable prices which match the scale of the system (see the first embodiment in the specification).

Brant, however, discloses a disk array controller comprising a channel interface device, a disk interface device and a memory device, wherein connections are made between the channel interface device and the memory device, and between the disk interface device and the memory device by PCI buses or other paths (see Figs. 1, 3, col. 5, lines 17-56 in Brant). Thus, Brant merely discloses logical components and logical connections. Brant does not disclose the physical components such as "package", and/or "platter" and "cable" as recited in the claims. Furthermore, Brant does not disclose the advantageous features of the present invention of making connections by "cables".

Therefore, the features of the present invention as recited in claims 13, 18, 22, 27, 30, 37 and 42 are not anticipated nor rendered obvious by Brant.

The above noted arguments presented with respect to claims 1, 8, 13, 18, 22, 27, 30, 37 and 42 apply as well to the remaining claims 2-12, 14, 15, 19, 20, 23-29 and 31 since these claims variously depend from claims 1, 8, 13, 18, 22, 27, 30, 37 and 42.

Therefore, based on the above, Applicants submit that the features of the present invention as recited in claims 1-15, 18-20, 22-31, 37 and 42 are not taught or suggested by Brant whether taken individually or in combination any of the other

references of record. Accordingly, reconsideration and withdrawal of the above described rejection of claims 1-15, 18-20, 22-31, 37 and 42 under 35 USC §102(b) as being anticipated by Brant is respectfully requested.

Claims 16, 21, 36, 38, 39 and 41 stand rejected under 35 USC §103(a) as being unpatentable over Brant. This rejection is traversed for the following reasons. Applicants submit that the features of the present invention as now recited in claims 16, 21, 36, 38, 39 and 41 are not taught or suggested by Brant whether taken individually or in combination any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

The features of the present invention as recited in claims 16, 21, 36, 38, 39 and 41 are not taught or suggested by Brant. In fact, since claims 16 and 21 depend from the above described claims 13 and 18, the above described arguments presented with respect to claims 13 and 18 apply as well to the use of Brant to reject claims 16 and 21. Therefore, Applicants submit that the features of the present invention as recited in claims 16 and 21 are not taught or suggested by Brant whether taken individually or in combination with any of the other references of record.

With respect to the remaining claims 36, 38, 39 and 41, Applicants submit that the features of the present invention as now recited in these claims are also not taught or suggested by Brant. Claims 36, 38, 39 and 41 are directed to a disk array controller comprising a channel interface package, a disk interface package, a memory package, and plural platters on which one or plurality of the packages are

mounted, wherein connections are made between the platters by cables, and wherein the path coupling the package to the cable is printed on each of the platters. The "package" means the circuit board on which a channel interface module or a disk interface module or memory module is mounted respectively. The "platter" means the circuit board on which connectors to the packages are mounted, and on which the paths coupling these packages are printed, and further on which a connector to the cable for coupling to another platter is mounted. Since the connections are made by cables, even if one platter fails, only components for which the packages mounted on that platter are responsible have to be stopped and the defective part on the platter can be replaced without stopping the entire system. Thus, faults can be remedied without stopping the system so that the system can be operated without interruption around the clock, all the year round. Furthermore, to cope with an increase or decrease in the number of platters bearing interface packages, the performance of internal buses can be made scalable. Therefore, scalability of performance and capacity is assured to suit a wide range of systems from small to large systems without unfavorably affecting the cost performance. Further, it becomes possible to supply products at reasonable prices which match the scale of the system (see the first embodiment in the specification).

Brant, however, discloses a disk array controller comprising a channel interface device, a disk interface device and a memory device, wherein connections are made between the channel interface device and the memory device, and between the disk interface device and the memory device by PCI buses or other paths (see Figs. 1, 3; col. 5, lines 17-56 in Brant). Thus, Brant merely discloses

logical components and logical connections. Brant does not disclose the physical components such as "package", "platter" and/or "cable" as recited in the claims. Furthermore, Brant does not disclose the advantageous features of the present invention of making connections by "cables".

Therefore, as per the above, it is quite clear that the features of the present invention as recited in claims 16, 21, 36, 38, 39 and 41 are not taught or suggested by Brant whether taken individually or in combination any of the other references of record.

Accordingly, reconsideration and withdrawal of the above described rejection of claims 16, 21, 36, 38, 39 and 41 under 35 USC §103(a) as being unpatentable over Brant is respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the reference utilized in the rejection of claims 1-16, 18-31, 36-39, 41 and 42.

In view of the foregoing amendments and remarks, Applicants submit that claims 1-16, 18-31, 36-39, 41 and 42 are in condition for allowance. Accordingly, early allowance of claims 1-16, 18-31, 36-39, 41 and 42 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (501.39293X00).

Respectfully submitted,

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